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ELECTRONIC PROPERTIES OF VERY THIN NATIVE SiO_2/a-Si:H INTERFACES AND THEIR COMPARISON WITH THOSE PREPARED BY BOTH DIELECTRIC BARRIER DISCHARGE OXIDATION AT ATMOSPHERIC PRESSURE AND BY CHEMICAL OXIDATION[1]

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The contribution deals with electronic properties of thin oxide/amorphous hydrogenated silicon (a-Si:H) measured by capacitance-voltage (C-V) and charge version of deep level transient spectroscopy (Q-DLTS). The interest was focused on the studies of the interface properties of very thin dielectrics formed by dielectric barrier discharge (DBD) or natively on the a-Si:H layer. These properties were compared with those of oxide layers prepared by chemical oxidation in HNO_3. The DBD was used for the preparation of a very thin SiO_2 layer on a-Si:H for the first time to our knowledge. Preliminary electrical measurements confirmed that a very low interface states density was detected in the case of the native oxide/a-Si:H and DBD oxide/a-Si:H.

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1 Introduction

Silicon is widely used in microelectronics as a substrate (c-Si) and silicon oxides as insulation layers. Because of a fast and cheep production, silicon in amorphous state (a-Si) is used in hydrogenised form (a-Si:H) for production of solar cells and thin film transistors (TFT). The a-Si:H can be deposited on various substrates mainly by Plasma Enhanced Chemical Vapor Deposition (PECVD). Silicon oxide can be produced by several techniques, such as oxygen plasma immersion ion implantation [1], chemical oxidation by HNO_3 [2], monoenergetical Ar^+ ion beam treatment followed by an exposure to oxygen [3], etc. Another possibility is to expose a prepared

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a-Si:H layer to air and the thin native SiO_2 is consequently formed on the surface. Additional technique is based on dielectric barrier discharge (DBD) [4].

To improve electrical parameters of solar cells and TFT, the SiO_2/a-Si:H structures are intensely studied at present time. This paper is devoted to investigation of some parameters of SiO_2/a-Si:H structures (interface states density, oxide layer thickness, form of built-in charge). SiO_2 layers were prepared by the chemical oxidation, native oxidation and DBD oxidation. DBD was used for SiO_2 layer preparation on a-Si:H for the first time and it was compared with chemical and native oxides. The properties of interfaces and oxide layers were measured by the C-V and Q-DLTS techniques.

2 Experiment

All the oxide layers were prepared on undoped a-Si:H layers $\sim$ 0.5 μm thick prepared by PE CVD technique at 13.56 MHz from a mixture of SiH_4 (10 sccm) and H_2 (90 sccm) gases by pressure 120 Pa, power 0.03 W cm^{-2}, sample temperature 160 °C and duration of deposition was 20 min.

Samples were exposed to ambient air after the deposition of a-Si:H layer and by this way at room temperature the native oxide layer of 1-2 nm thickness have grown. Abbreviation of the samples is "am3".

Other method for oxide preparation that was used is chemical oxidation. This method of low temperature oxidation by use of nitric acid, i.e. nitric acid oxidation of silicon (NAOS), has been developed in Osaka University [5, 6]. On the top of the a-Si:H surface, an oxide layer of 5-8 nm thickness was prepared in 68 % water solution of HNO_3 acid at boiling temperature (121°C) during 30 minutes. Abbreviation of the samples is "naos".

Additional type of oxide layer was prepared by DBD. Dielectric barrier discharges are characterized by discharge gaps and the presence of one or more insulating layers in between the gaps. Typical operation conditions are pressures between 10 and 1000 kPa and frequencies in the range of 50 Hz to 100 kHz. Three basic configurations to produce DBDs can be distinguished, the volume discharge, the surface discharge and the coplanar discharge arrangement. The volume discharge arrangement is most common. It consists in general of a gas gap between parallel electrode plates with one or both electrodes covered by a dielectric layer. The ignition voltage is mainly determined by the size of the gap, the kind of gas and its pressure.

Surface discharge arrangement consists of one or more long high voltage electrodes on the surface of a dielectric and an extended counter electrode on its reverse side. Pure surface discharges appear on the surface of the dielectric. The discharge ignites at Paschen minimum conditions. Its area on the surface is proportional to the amplitude of the applied voltage.

The coplanar discharge arrangement on the other hand consists of pair(s) of extended electrodes that are embedded in a dielectric close its surface. Most often the electrode separation is in the order of 100 μm. The discharge occurs on the surface of the dielectric in between the location of the electrodes.

In our experiments with utilization of DBD for a-Si:H surface exposure the coplanar discharge arangement has been used with following parameters:

Frequency: 14 kHz; voltage: 7 kV, distance of electrodes: 0.5 mm; width of electrodes: 1.65 mm; material of dielectrics: Al_2O_3 based.

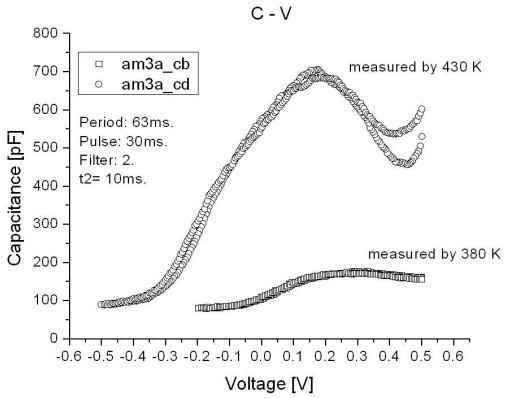

Fig. 1. C-V record of structure native oxide/a-Si:H/c-Si measured with various bias voltages by 380 K and 430 K.

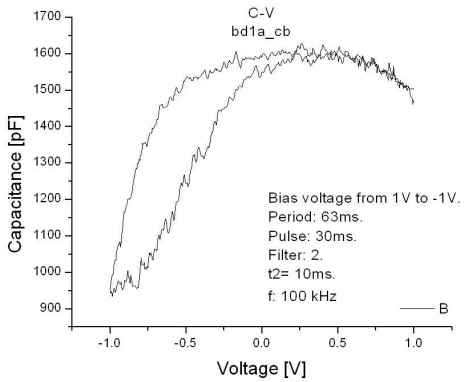

Fig. 2. C-V record of structure DBD oxide/a-Si:H/c-Si. Plasma exposure time: 30 s.

Pressure 133 kPa of O_2 at flow regime was used during the experiment. Distance of sample from the surface of dielectric was 0.25 mm. Time of exposure was 30 s (bd1) and 60 s (bd2), respectively. The samples were exposed at room temperature. Abbreviation of the samples was "bd1", "bd2" according to time of exposure (see FigsG. 2, 3, 5, 6).

The samples were treated using a atmospheric plasma source which is a modification of the surface-dielectric-barier-discharge plasma source described in details in reference [7].

3 Measurements

There was a C-V measurement at $\approx$ 100 kHz and Charge version of Deep Level Transient Spectroscopy (Q-DLTS) using a spectrometer developed at the Institute of Physics of SAS [3, 8] used to characterize the prepared samples. Both measurements were realized with the same measurement equipment in the same cryostat. Q-DLTS was measured by the voltage steps of 1V, 4V, 6V, (Fig. 4, 5 and 6) and by 0.2V in the case of the structures with chemical oxides (Fig. 7 and 8).

4 Results

Main results concern the behavior of the Q-DLTS spectra and the C-V characteristics.

i. Accumulation capacitance was not reached under given conditions for the samples with native oxides (Fig. 1, the corresponding capacitance is very low) whereas for DBD oxides (see Fig. 2, 3), the accumulation was observed. From the hysteresis on Fig. 2 and 3, it can be deduced the presence of a mobile charge in oxide layer which is not observed for the native oxide. The results indicate that the DBD and chemical oxidations influence also the bulk of the a-Si:H layer, not only the oxide/a-Si:H interface.

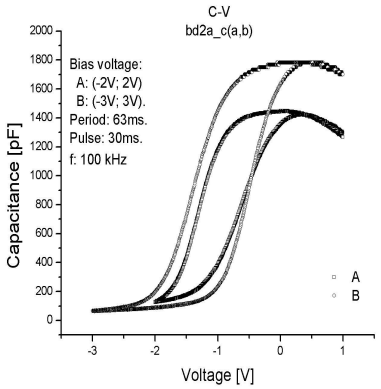

Fig. 3. C-V record of structure DBD oxide/a-Si:H/c-Si by various bias voltages. Exposure time: 60 s.

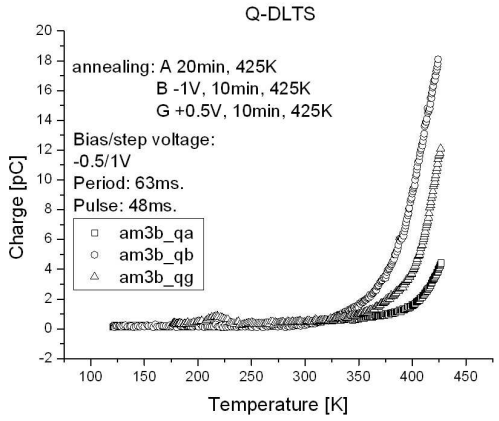

Fig. 4. Q-DLTS spectra of the structure native oxide/a-Si:H/c-Si annealed under various conditions according picture label.

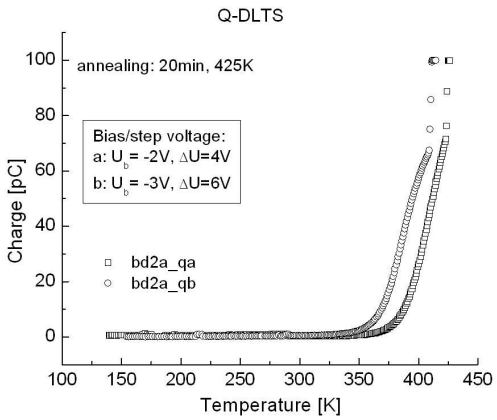

Fig. 5. Q-DLTS spectra of the structure with DBD oxide/a-Si:H/c-Si annealed 20 min by 425K and measured by various conditions. Preparation time of the oxide: 60 s.

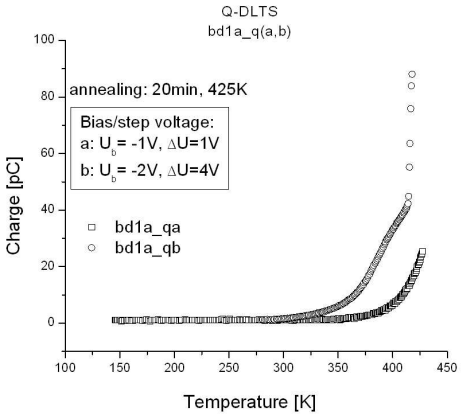

Fig. 6. Q-DLTS spectra of the structure with DBD oxide/a-Si:H/c-Si annealed 20 min by 425K and measured by various conditions. Preparation time of the oxide: 30 s.

ii. A "standard" behaviour of deep level spectra (according Powel and Dean model [9, 10]) was measured on the samples with the chemical oxide layer (see Fig. 7 and 8). However, only two distinct dangling bond components (at lower temperatures) could be identified, namely D_h at 320 K and D_z at 390 K at the rate window of 100 s^{-1}, similarly as in [3]. The structures had an increased conductivity at higher temperatures.

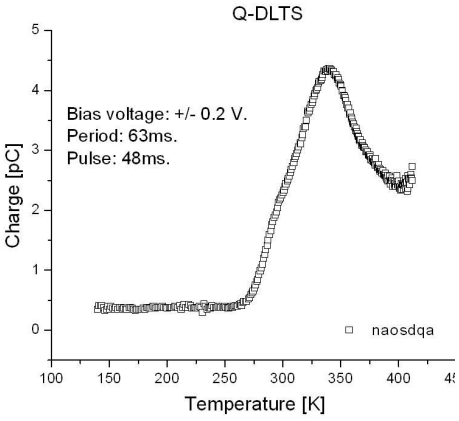

Fig. 7. Q-DLTS spectra of the structure with chemically formed oxide/a-Si:H/c-Si.

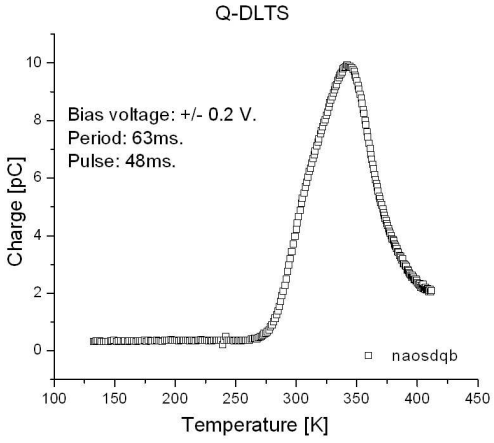

Fig. 8. Q-DLTS spectra of structure with chemically formed oxide/a-Si:H/c-Si. Bias annealing at 420 K.

iii. Interface properties investigated by Q-DLTS indicate that the native oxide layer/a-Si:H and DBD oxide/a-Si:H are without remarkable signal coming of the deep states (Fig. 4, 5 and 6) comparing to the MIS structures with the chemical oxide. The absence of the signal is caused probably by the preparation properties.

iv. It is possible to redistribute such a type of deep local states as it can be seen in the case of chemical oxides by a "bias annealing" (see Fig. 8) at –1V (+0.5V), 380K (425K) for 10 min. It was impossible with the samples with the native oxide and DBD oxide layers (see Figs. 4, 5 and 6).

5 Conclusion

The interest was focused on the experimental research of the interface properties of very thin dielectrics formed natively on the a-Si:H surface after the PECVD of 1 μm thick a-Si:H layer grown at 250 °C on a crystalline Si substrate, DBD oxide/a-Si:H and chemical oxide/a-Si:H structures.

The deep level spectra have been analyzed and compared with previous results published and interpreted on the basis of the Powell-Dean theoretical model.

We compare the results obtained on the very thin SiO_2/a-Si:H structure prepared by the oxidation using DBD at atmospheric pressure in oxygen with the chemical and native oxides. The DBD technique was used for a very thin SiO_2 layer formation on a-Si:H for the first time to our knowledge,.

The preliminary electrical measurements confirmed that a very low density of interface states was detected in the cases of the native oxide/a-Si:H and DBD oxide/a-Si:H. Relying on Q-DLTS we suppose that a a-Si:H layer was partly transformed into a Si micro-crystalline-like layer during

the preparation of a very thin oxide layer and consequently the "standard" distribution of the a-Si:H deep states was not measured. On the other hand, the Q-DLTS spectra do not contain any signal confirming existence of deep states in the band gap of the semiconductor in 100 – 350 K region. Other parameters concerning the electrical quality of the dielectric layers also indicate that such a type of the SiO_2 layers prepared by the DBD technique can be applied in sub-micron technology, e.g. for production the MOS based devices.

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