

**ELECTRICAL BEHAVIOUR OF SPUTTERED Al/SiGe/Si STRUCTURES<sup>1</sup>****Zs. J. Horváth<sup>a,2</sup>, M. Serényi<sup>a</sup>, M. Ádám<sup>a</sup>, I. Szabó<sup>a</sup>, V. Rakovics<sup>a</sup>, P. Turmezei<sup>b</sup>,  
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The current-voltage and capacitance-voltage behaviour of amorphous SiGe layers sputtered onto p-type Si substrates, have been studied in the temperature range of 80-320 K by using Al Schottky contacts as test structures. Although a significant influence of the preparation conditions was obtained on the electrical behaviour of the structures, they exhibited similar specific features of the electrical characteristics. These features are mainly due to deep energy states which are present in the sputtered layers and at the amorphous/crystalline interface.

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**1 Introduction**

During the last two decades amorphous SiGe became an important material for solar cells, light emitting diodes, and thin film transistors in flat panel displays [1, 2]. In this work amorphous SiGe layers were grown on p-type Si substrates by RF magnetron sputtering. Al Schottky contacts were prepared to the obtained a-SiGe/c-Si structures, and their vertical electrical characteristics were studied by current-voltage (I-V) and capacitance-voltage (C-V) measurements. The effects of the chemical treatment of Si surface before sputtering, and of the hydrogenation of the SiGe layer were studied.

**2 Experimental**

The amorphous SiGe layers with a thickness of 900 nm were sputtered from a SiGe polycrystalline target on p-type Si substrates with a nominal resistivity of 6  $\Omega$  cm (nominal doping level of about  $2 \times 10^{15}$  cm<sup>-3</sup>) at a frequency of 13.6 MHz and bias of 1.5 kV in Ar<sup>+</sup> plasma at pressure of  $2.0 \times 10^{-3}$  mbar at room temperature. The Ge content of the target was about 6%, but due to the Rutherford backscattering measurements performed on the samples prepared similarly, the Ge content in the sputtered films was 4% only.

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Tab. 1. The apparent barrier height and the ideality factor obtained from the room temperature current-voltage measurements as a function of the surface treatment of the substrates before sputtering for the structures without hydrogenation.

Wafer	Surface treatment	$\Phi_{bI}$ , eV	n
S3P	Aceton	$0.68 \pm 0.01$	$5.1 \pm 0.2$
S4P	HF	$0.68 \pm 0.01$	$1.10 \pm 0.01$

Two different methods were used for the treatment of Si surface before sputtering. The "Acetone" treatment (see Table 1) was performed by boiling the wafer in clean acetone three times consecutively for 5 min each. The "HF" treatment consisted of two steps: 1) Cleaning in 1:1 solution of  $H_2SO_4$  and  $H_2O_2$  for 30 min. 2) Etch in 1:20 solution of HF and  $H_2O$  for 1 min [3].

The effect of hydrogenation was also studied introducing 0.4 %  $H^+$  into the plasma during deposition [4]. These structures were prepared using "Acetone" treatment before sputtering.

Al was evaporated on both the front and backside of the wafers for the formation of Schottky and ohmic contacts, respectively. Square diodes with an area of  $0.64 \text{ mm}^2$  were formed on the front side of the wafers by standard photolithography.

I-V and 1 MHz C-V measurements were carried out at room temperature (10 diodes per wafer) and in the temperature range of 80-320 K (2-4 diodes per wafer) in dark. The room temperature I-V characteristics were evaluated for the thermionic emission theory using an effective Richardson constant of  $32 \text{ Acm}^{-2}\text{K}^{-2}$ , characteristic for p-Si [5].

### 3 Results and discussion

Although significant influence of the preparation conditions was obtained on the electrical behaviour of the structures, the structures exhibited similar specific features. As a common picture, forward I-V characteristics consisted of four different parts as shown in Figs. 1 and 2. for wafers S3P and S4P ("Aceton" and "HF" treatments, respectively). The central, most abrupt part of the I-V characteristics is attributed to a Schottky barrier formed by Al on the sputtered layers. The first part at low biases showed ohmic behaviour, and it is connected with a parallel conductance due to hopping current mechanism through the amorphous SiGe layer. In the third part exhibiting a linear  $\log I$ -V relationship with a lower slope at relatively high biases, the current is limited by space charges in the SiGe layer, while in the fourth part at high biases, the current is limited by the series resistance. The different parts of the forward I-V characteristics appeared at different temperatures for the different structures, as it can be seen in Figs. 1 and 2. Similar behaviour was obtained recently in structures with amorphous Si/Ge multilayers also grown on p-Si [6].

The apparent barrier height and ideality factor evaluated from the room temperature I-V characteristics of samples without hydrogenation, are presented in Table 1. The sample with "Acetone" treatment exhibited very high ideality factor of  $5.1 \pm 0.2$ . This is connected with that its I-V behaviour was limited at room temperature by the transport through the sputtered layer due to space charge limited current mechanism (third part of characteristics in Figs. 1 and 2).

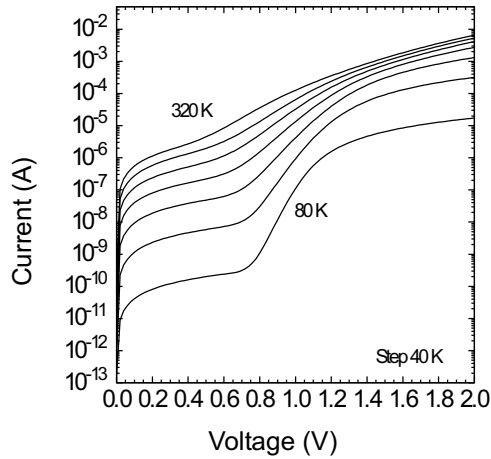


Fig. 1. Typical forward current-voltage characteristics of Al/SiGe/p-Si structures "S3P" prepared with "Aceton" surface treatment.

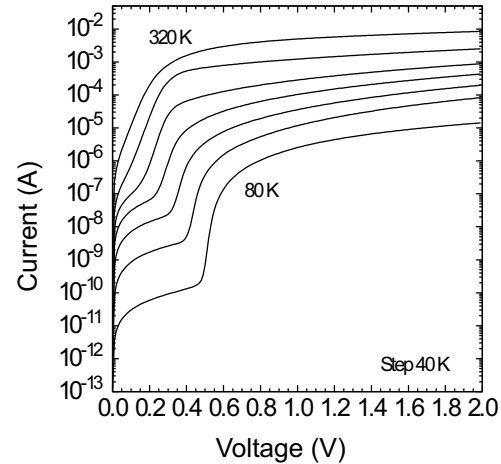


Fig. 2. Typical forward current-voltage characteristics of Al/SiGe/p-Si structures "S4P" prepared with "HF" surface treatment.

For sample with "HF" treatment very good ideality factor of  $1.10 \pm 0.01$  was obtained.

Although the apparent barrier height values were 0.68 eV for both treatments, the change of the surface preparation from "Aceton" to "HF" treatment affected the I-V characteristics significantly, as it can be seen comparing Figs. 1 and 2. As mentioned above, the "HF" treatment decreased also the ideality factor significantly. This indicates that the "HF" treatment yielded much better interface between the Si substrate and the sputtered SiGe layer with much lower energy barrier, than the "Aceton" treatment. The high ideality factors and the less abrupt I-V characteristics for "Acetone" treatment (see Table 1 and Figs. 1 and 2) are connected with the drop of the applied bias at the SiGe/Si interface in these structures.

The hydrogenated amorphous structures prepared exhibited I-V characteristics depending on the temperature very weakly [4], as presented in Fig. 3. At low current levels there is an exponential I-V relationship, which saturates at higher current levels. This exponential I-V dependence at low biases is considered to be contact limited. The saturating part of the forward I-V characteristics exhibits a quadratic dependence of the current on the bias, as presented in Fig. 4, indicating space-charge limited currents [2, 4, 7–10].

The C-V characteristics of the structures also exhibited specific behaviour. They showed strong temperature dependence, as presented in Fig. 5 for wafer "S4P" ("HF" surface treatment). This feature is connected with the recharging response of deep energy states present in the amorphous layer which yields large excess capacitance [2]. The higher the temperature the faster the recharging response of deep levels that results in higher capacitance at higher temperatures at the measurement frequency of 1 MHz. Due to the contribution of deep levels, the evaluated apparent free hole concentration is in the range of  $2 \times 10^{15}$ – $2 \times 10^{16}$  cm<sup>-3</sup>, depending on the bias and temperature, as presented in Fig. 6 for structures "S3P" ("Aceton" surface treatment). The lower edge of this concentration range corresponds to the nominal resistivity of the substrate of 6 Ωcm.

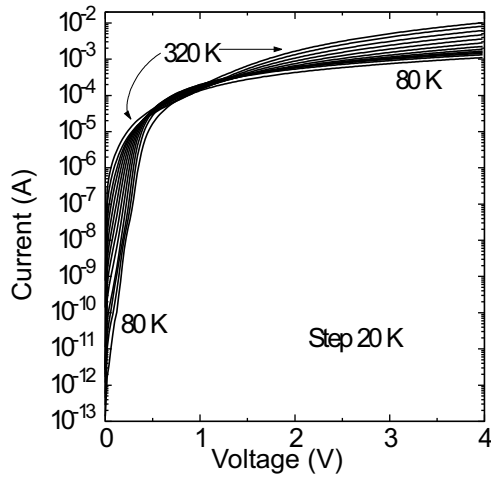


Fig. 3. Typical current-voltage characteristics of the Al/SiGe/p-Si structures "SSP" prepared with Ar<sup>+</sup> plasma with 0.4% H<sup>+</sup> content ("Aceton" surface treatment).

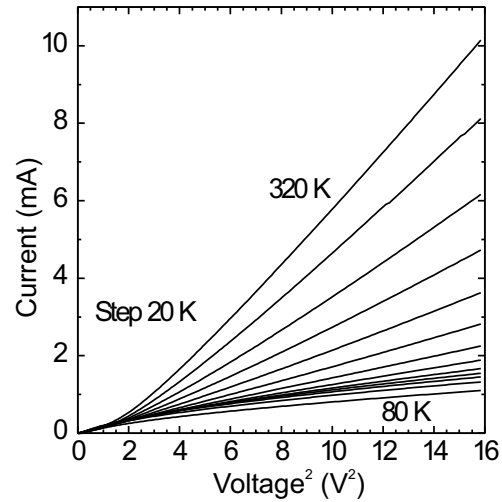


Fig. 4. The  $I$  vs.  $V^2$  plot of the current-voltage characteristics presented in Fig. 3 for a hydrogenated Al/SiGe/p-Si structure.

Further on, C-V characteristics exhibited a peak for positive forward biases at low temperatures, as it is shown in Fig. 5, which is not observed for usual Schottky junctions. This phenomenon can be connected with the fast change of the phase shift between the current and voltage of the 1 MHz measuring signal, when the current suddenly increases with increasing forward bias [2]. On the other hand, the capacitance peak may also be due to deep levels or interface states in the SiGe layer or at the SiGe/Si interface [11, 12].

#### 4 Conclusions

The current-voltage and capacitance-voltage behaviour of amorphous SiGe layers sputtered onto p-type Si substrates have been studied in the temperature range of 80-320 K by using Al Schottky contacts as test structures. A significant influence of the preparation circumstances of the layers has been obtained on the electrical behaviour of the structures. However, the structures exhibited similar specific features. Forward I-V characteristics consisted of four different parts corresponding to different current mechanisms. C-V characteristics exhibited excess capacitance, connected with deep levels in the sputtered layers.

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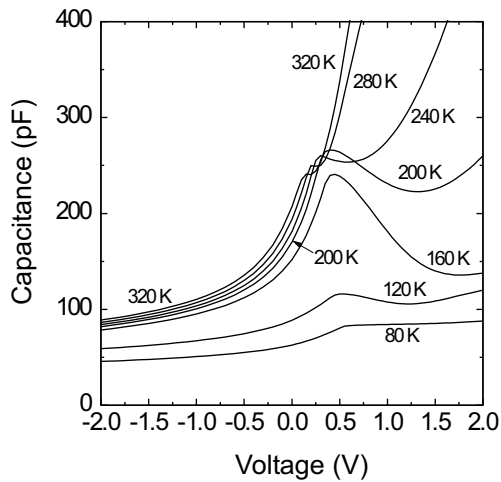


Fig. 5. Typical capacitance-voltage characteristics of Al/SiGe/p-Si structures "S4P" ("HF" surface treatment).

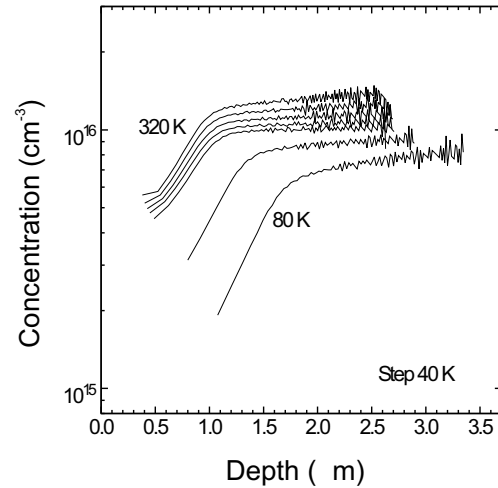


Fig. 6. The apparent free hole concentration as a function of the apparent depth from the Al/SiGe interface, evaluated from the capacitance-voltage characteristics of Al/SiGe/p-Si structures "S3P" ("Aceton" surface treatment).

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