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REAR-SURFACE PASSIVATION AND DESIGN FOR THIN p-TYPE MULTICRYSTALLINE SILICON SOLAR CELLS *

S. De Wolf[1] †, G. Agostinelli, H.F.W. Dekkers, J. Szlufcik
IMEC vzw, Kapeldreef 75, B-3001 Leuven, Belgium
† *Also with E.E. Dept., Katholieke Universiteit Leuven, B-3001 Leuven, Belgium*

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Recently, an important trend within crystalline silicon solar cell processing is the assignment of a more prominent role to thin ($\leq$150μm) substrates. This considerably reduces dominant material costs, albeit at the expense of giving up well-established solar cell processing steps, such as the screenprinted aluminium back-surface-field (BSF) and contact formation, due to excessive warping of the cells. Next to this, thinner wafers evidently increase the need for excellent rear-surface passivation-schemes. Finally, it is generally accepted that when using multicrystalline Si (mc-Si) substrates, dedicated processing-steps are essential to upgrade the average minority charge carrier lifetime in the bulk, τ_{bulk}. Generally, this is done by applying gettering and/or hydrogenation-steps, both being relatively high temperature steps. Futhermore, for such thin solar cells, to be sufficiently efficient, the minority charge carrier diffusion length in the bulk, L_{bulk}, should exceed twice the waferthickness.

This paper describes a solar cell processing route potentially overcoming all three constraints as pointed out on thin p-type mc-Si silicon substrates. It will be shown that the use of POCl$_3$-diffusion is rather essential to increase τ_{bulk}. For the rear side, it is then shown that direct Plasma Enhanced Chemical Vapour Deposited (PECVD) a-Si:H layers can yield surface recombination velocities with values below 1.5m.s^{-1}. This is achieved throughout a broad excess minority charge carrier density, Δn, range of about 5x10^{18} to 5x10^{22}m^{-3}, for 20nm thick intrinsic PECVD a-Si layers on top of 1.0x10$^{-2}\Omega$.m p-type Float Zone (FZ) silicon wafers. Finally, results are given of subsequent POCl$_3$ gettering and PECVD a-Si:H surface passivation throughout a complete cast mc-Si Polix 1.0x10$^{-2}\Omega$.m p-type ingot by means of L_{eff} extraction.

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1 Introduction

A typical efficient low-cost solar cell process based on standard mc-Si substrates (resistivity: $\sim$1.0x10$^{-2}\Omega$.m, p-type; thickness: 300 – 350μm, area $\geq$ 100x100mm^2) consists of a few well-established steps, in a subsequent order:

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[1] E-mail address: stefaan.dewolf@imec.be

- Acidic isotropic texturing. This ‘surface roughening’ replaces the classic, but less effective alkaline texturing based on NaOH or KOH etching. Synchronically, this step removes the wire-saw damage, present upon wafering from cast ingots [1].
- High quality homogeneous emitter $POCl_3$ diffusion, with a good response for short wavelength photons (sheet resistances of 50 - 60Ω/sq).
- Parasitic edge junction removal by dry plasma-etching.
- Anti-reflective coating (ARC) deposition of hydrogen-saturated direct PECVD SiN_X:H layers on the front side of the samples.
- Screenprinted metallisation of the electrical front and rear contacts, by respectively using Ag and Al based organic metallisation pastes. This step is then typically followed by a short high temperature step: contact firing.

Within this technological frame, energy conversion efficiencies of up to 16.5% under an AM1.5, 1kW.m^{-2} illumination spectrum have been achieved on cell-level for 125x125mm^2 substrates, with corresponding maximum power outputs of up to 89.9W on a 36 cell module-level [2]. However, an important drawback present within this approach is the still dominating wafer-cost on module-level [3]. Hence, the important general trend to assign a more prominent role to thin ($\leq 150\mu$m) substrates within crystalline Si solar cell processing, which naturally increases the wafering yield [4].

As general rules of thumb, it can be stated that to obtain efficient thin solar cells, on one hand the bulk minority charge carrier diffusion-length, L_{bulk}, should exceed twice the wafer thickness. On the other hand an excellent rear-surface passivation should be provided with effective surface recombination velocities, S_{eff}, of about 1m.s^{-1} [5].

2 Lifetime improvement on multicrystalline Si

For mc-Si solar cell processing, the shift towards thinner wafers represents a technological issue, since it is generally assumed that τ_{bulk} in the material still needs to be considerably enhanced within the cell process itself. Two basics τ_{bulk} enhancing mechanisms are believed to be at work during the simple processing-scheme as shown before: gettering and defect-passivation by hydrogenation, both being relatively high temperature steps.

Apart from the excellent surface passivation properties direct PECVD SiN_X:H films provide upon contact firing, this thermal treatment is believed to be able to release hydrogen atoms into the Si bulk from these layers. Especially the electrical quality of the grainboundaries has been shown on Light Beam Induced Current (LBIC) maps to be improved within this approach. The exact role played by the screenprinted Al layer on the rearside, and more specifically the presumed synergetic hydrogenating effect it leads to during contact firing, as seen on e.g. Si ribbons, is still under debate [6–8]. However, thin substrates do not allow the use of such screenprinted Al layers. The most evident reason is that because of the significant differences in thermal expansion coefficients between Si (7.6x10^{-6} K^{-1}) and Al (23.9x10^{-6} K^{-1}), excessive substrate warping is experienced during contact firing [9]. Secondly, the rather high values for S_{eff} and the poor light-reflecting properties, typical for such layers is believed to be unacceptable for high-efficiency cell processing.

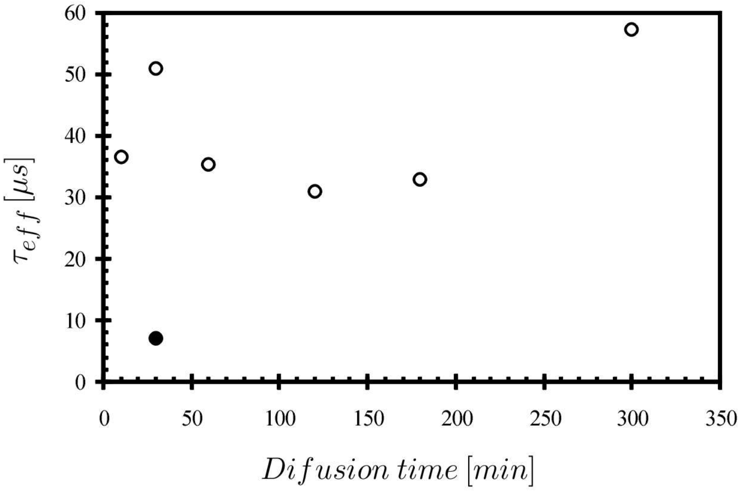

Fig. 1. $\tau_{eff}(\Delta n \sim 10^{20}\text{m}^{-3})$ for adjacent p-type mc-Si 1Ω.cm substrates after POCl$_3$ diffusion and subsequent 'emitter' etch-off. Surface passivation is provided by thermally treated direct PECVD SiN$_x$:H. Full circle denotes sample with identical thermal history as for standard front-emitter diffusion, but without doping gasses present during annealing.

Prolonged POCl$_3$ diffusion is known for its ability to improve τ_{bulk} to a great extent for mc-Si due to gettering [10]. In Fig. 1, τ_{eff} as function of the POCl$_3$ diffusion time is given at values for Δn of 10^{20}m^{-3}. These lifetimes are measured with a quasi-steady-state photoconductance (QSSPC) system, where a slow decaying flashlight allows the measurement of τ_{eff} as function of Δn [11]. The samples shown were all adjacent, originating from a 1x$10^{-2}\Omega$.m mc-Si Polix ingot, and with a thickness of about 300μm. Upon POCl$_3$ diffusion, and subsequent diffusion-glass removal (10%HF), the emitters were etched off in a CP4 solution (HNO$_3$:CH$_3$COOH:HF 15:8:5). Surface passivation was then provided by thermally treated direct PECVD SiN$_X$:H deposition. The thermal reference given in the graph has exactly the same thermal history as for samples with standard emitter POCl$_3$ diffusion conditions, but evidently without doping gasses present during the annealing process.

Fig. 1 shows that for commercially available mc-Si material, even for very short diffusion-times in the order of a few minutes, an important increase in τ_{eff} can be achieved,compared to the thermal reference. This corresponds with values for L_{eff} exceeding 300μm. Interestingly, at about standard emitter POCl$_3$ diffusion conditions, τ_{eff} tends to show a local maximum, whereupon it again decreases. For longer diffusion times, however, the value for τ_{eff} seems to improve again. The presence of this maximum has been explained in terms of a trade-off between phosphorous gettering and thermal degradation in mc-Si material. The physical cause of the thermal degradation has by some authors been attributed to an increase in dislocation density due to high temperature oxidations [12]. Others have suggested in the past that the cause of this thermal degradation is to be found in the dissociation of impurity precipitates, resulting in a greater concentration of more harmful interstitial impurities [13]. Within the latter frame, it would be possible to explain why longer diffusion times apparently allow for a more complete gettering of all released impurity atoms, as is suggested by the measured data. In any case, Fig. 1 makes it clear why it is very advantageous to use $POCl_3$ diffusions for emitter formation in mc-Si material, and explains the difficulties expected when applying a full low-temperature ($T_{process} < 300\,^{\circ}\mathrm{C}$) processing scheme, such as that for a-Si:H / c-Si heterojunction emitter cells, on mc-Si substrates.

3 Rear-surface passivation

As pointed out before, thinner wafers evidently increase the need for excellent rear-surface passivation-schemes. Several different approaches to yield low values for S_{eff} have been developed over the years, including thermally grown and plasma deposited silicon oxides (SiO_2) [14, 15], remote PECVD SiN_X films [16], doped and/or intrinsic PECVD amorphous or microcrystalline silicon layers (a-Si:H or μ-Si:H) [17] and PECVD amorphous SiC_X:H films [18]. Moreover, since the application of thin substrates makes it impossible to continue to use fired screenprinted Al layers for back-contact and back surface field (BSF) formation, it can be understood there exists as well a need for excellent alternative contacting schemes at the backside of the cells. A drawback present when using of PECVD SiN_X films at the rear is that parasitic shunting occurs between the rear metal contact and negatively charged inversion layer that is created due to the presence of fixed positive charges within the SiN_X films. This phenomenon deteriorates the overall cell performance [19]. This is not the case when applying a-Si:H layers for surface-passivation. These layers can easily be boron–doped for BSF formation. In this way they permit the avoidance of making a direct metallic, and usually highly recombinative, contact with the electrically active layer.

In Fig. 2, it is shown how for the rear side passivation, the application of 20nm thick direct PECVD a-Si:H layers can yield high values for τ_{eff}. The used sample, with a thickness of 260μm, originates from a high quality FZ monocrystalline p-type 1x10$^{-2}\Omega$.m ingot and was cleaned prior the depositions in a H_2O_2:H_2SO_4 solution, followed by rinsing and an HF-dip. Within these measurements, it is assumed that generation and recombination in thin a-Si layers can be neglected, thus these films are considered as surface-passivating layers for crystalline wafers. Moreover, the figure shows the typical dependence of τ_{eff} on Δn, as is measured by the QSSPC technique. This stresses the importance to mention at what value for Δn, τ_{eff} is exactly measured. Since under an AM1.5, 1kW.m^{-2} illumination spectrum, the injection level for a standard solar cell as described before is in a range of about 8.0x10^{18} to 2.0x10^{20}m^{-3} (for respectively the short circuit current density J_{sc} and the open circuit voltage V_{oc} in a cell with L_{bulk} = 250μm), evidently one should focus on this region in the graph. However, at low Δn values, measurements often suffer from erroneously high registered values for τ_{eff}, making interpretations cumbersome. This phenomenon is considered to be a measurement artefact that is caused by shallow trapping effects in the sample [20]. The peak at a Δn value of about the background doping density of the substrate is typical for a Shockley-Read-Hall type of recombination mechanism. Once past this value, one enters the region of high injection where Auger recombination starts to prevail. The second curve in Fig. 2 gives the calculated S_{eff}. The relation between this parameter, τ_{eff} and τ_{bulk}, in case of a sample with two identically treated

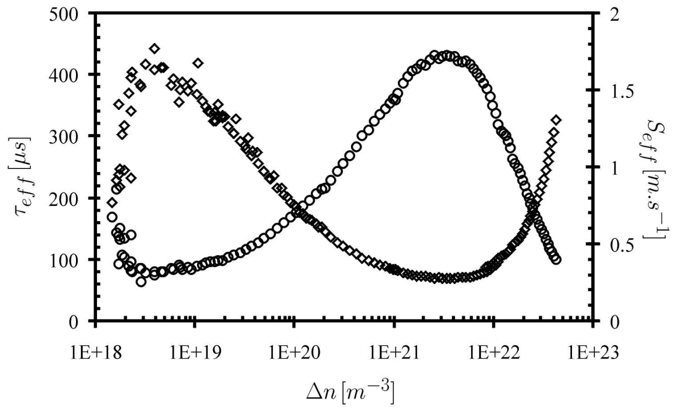

Fig. 2. τ_{eff} (Circles) and S_{eff} (Diamonds) versus Δn for a p-type FZ 1Ω.cm substrate. The surface-passivation (both sides) was provided by direct PECVD intrinsic a-Si layers (thickness ~ 20nm).

surfaces, is given by the formula [21]:

$$S_{eff} = \sqrt{D_a\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right)}\tan\left[\frac{W}{2}\sqrt{\frac{1}{D_a}\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right)}\right] \tag{1}$$

with the wafer thickness W and the ambipolar diffusion coefficient $D_a = (n+p)/(n/D_p + p/D_n)$. To avoid underestimations for the calculated values for S_{eff} in the figure, τ_{bulk} was set at infinite, therefore S_{eff} can be considered as being a worst case upper limit.

4 Results throughout a complete cast mc-Si ingot

An important question to be asked for low-cost cell processing is how these processing steps affect the wafer-quality throughout a complete cast ingot. In Fig. 3, it is shown how this kind of surface-passivation behaves when applied on Polix mc-Si samples of about 300μm thick, that were selected at regular intervals throughout a complete cast p-type 1Ω.cm ingot. After isotropic texturing, all samples underwent the standard emitter $POCl_3$ diffusion, as described before. Prior to the deposition of 20nm thick PECVD a-Si layers on both sides of the substrates, the emitter was etched off in a CP4 solution and the samples were cleaned in a H_2O_2:H_2SO_4 solution, followed by rinsing and an HF-dip. To discriminate between the surface-passivation and the bulk-improvement by $POCl_3$ gettering is rather cumbersome. However it can be seen that the combined effect leads to values for L_{eff} exceeding the for 150μm thick solar cells required 300μm in most parts of the ingot. These values are easily obtained through $L_{eff} = \sqrt{D.\tau_{eff}}$, where D

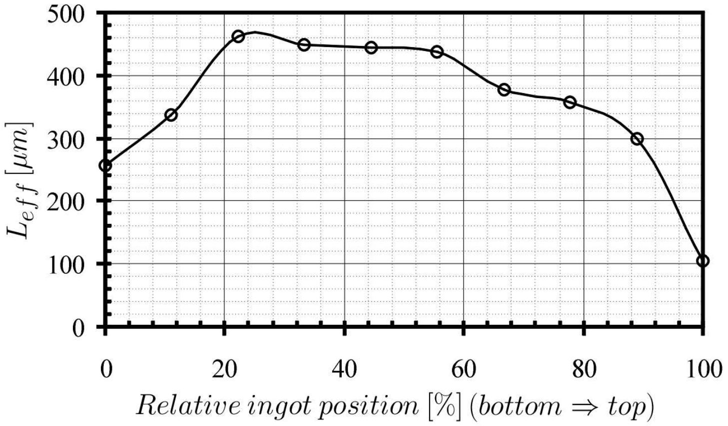

Fig. 3. L$_{eff}$(Δn $\sim$ 10^{20}m^{-3}) versus ingot position for a p-type 1x10^{-2}Ω.m Polix ingot. The surface-passivation (both sides) was provided by direct PECVD intrinsic a-Si layers (thickness $\sim$ 20nm).

is the diffusion constant, while τ_{eff} has been measured with the aforementioned QSSPC technique. The lower values at the bottom and the top of the ingot are typically described in terms of respectively a greater defect-density and impurity-segregation towards the top, thus reducing τ_{eff} [22].

5 Summary & conclusions

In this paper, it has been shown that the use of POCl$_3$-diffusion is rather essential to increase τ_{bulk} when one aims at manufacturing thin ($\leq$150μm) solar cells from p-type mc-Si substrates. Furthermore, for the rear side surface passivation, it has been shown that 20nm thick intrinsic direct PECVD a-Si:H layers on top of 1Ω.cm p-type FZ silicon wafers can yield values for S$_{eff}$ below 1.5m.s^{-1}, achieved throughout a broad range for the value of Δn range of about 5x10^{18} to 5x10^{22}m^{-3}, Finally, results have been given of subsequent POCl$_3$ gettering and PECVD a-Si:H surface passivation throughout a complete cast mc-Si Polix 1Ω.cm p-type ingot by means of L_{eff} extraction. Here it was seen that, apart from the far bottom and top of the ingot, the electrical bulk quality of all samples is improved by the given methods to values of L_{eff} exceeding the required 300μm.

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