

# THE INFLUENCE OF THE SiO<sub>2</sub> UNDERLAYER ON THE JOULE HEATING OF Al-Cu-Si METALLIZATION OF SILICON DEVICES

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Experimental conductors were patterned in Al-Cu-Si films deposited by magnetron sputtering onto oxidized silicon substrates with constant as well as with varying SiO<sub>2</sub> thicknesses. The stripes were stressed by high current density ( $> 10^6$  A/cm<sup>2</sup>). Under these conditions the temperature increase of the conductors due to Joule heating reached 70°C for the first type of substrate. For the substrate with varying oxide thickness, smaller than or equal to that in the previous case, the mean value of the temperature increase (fluctuating along the conductor) was 37–39°C. The experimental results are compared with calculations of temperature distribution based on a simple model. The agreement is quite good and it indicates that the heating of the metallization is influenced mainly by the thickness of the SiO<sub>2</sub> underlayer, which has the thermal conductivity by two orders of magnitude smaller than silicon. The results show that the Joule heating of conductors stressed by high current densities can significantly influence the operational conditions and reliability of semiconductor devices.

## 1. INTRODUCTION

Electromigration is an important degradation process which adversely influences the reliability and lifetime of the metallization of semiconductor devices. Among the reviews concerning this phenomenon at least that by d'Heurle and Ho should be mentioned [1].

The electromigration performance of the often used Al-Cu-Si conductors of silicon devices and circuits was studied in many papers (e.g. [2, 3, 4]). From our previous results [4, 5, 6] it follows that the Joule heating of Al-based metallization deposited onto a SiO<sub>2</sub> underlayer and stressed during the electromigration lifetime test by the current density  $j \geq 10^6$  A/cm<sup>2</sup> cannot be omitted. With the usual oxide thickness  $\approx 1$   $\mu$ m the temperature increase equals some tens of degrees. Consequently, the electromigration failure process is accelerated and the conductor lifetime decreases. The current densities of  $\geq 10^6$  A/cm<sup>2</sup> are

desirable for the operation of VLSI and ULSI circuits [7]. Therefore, some attention should be paid to this problem.

For the heating of metallization the thermal properties of semiconductor substrate, the insulating layers and package materials including the bond wires are important. From this point of view the high thermal conductivity  $\lambda_{Si} = 1.4$  W/cm K is the great advantage of silicon. It is comparable with the thermal conductivity of metals (e.g.  $\lambda_{Al} = 2.35$  W/cm K), being approx. by two orders of magnitude higher than that of SiO<sub>2</sub> ( $\lambda_{SiO_2} = 1.3 \times 10^{-2}$  W/cm K). Therefore, it can be expected that the thickness of SiO<sub>2</sub> will influence the heating of metallization considerably.

The above mentioned problem will be more serious in the case of advanced semiconductor structures based on new materials like GaAs or polyimide, which on the other hand possess smaller thermal conductivities.

In this paper the influence of the SiO<sub>2</sub> underlayer on the heating of Al-Cu-Si metallization is studied for two types of experimental structures.

## 2. EXPERIMENTAL DETAILS

Al-Cu-Si films 0.6  $\mu$ m thick were deposited by magnetron sputtering at the substrate temperature  $\leq 150^\circ$  C onto thermally oxidized silicon. The composition of the planar magnetron target was Al-4 wt. % Cu-1 wt. % Si. Two types of substrates were used: a) wafers with planar surface and with the constant oxide thickness  $t_{SiO_2} = 1.6$   $\mu$ m; b) wafers prepared by selective oxidation through a nitride mask with the SiO<sub>2</sub> thickness varying between 1.6 and 0.04  $\mu$ m. The "bird beaks" at the boundaries of thick and thin oxide regions were lowered to 0.3  $\mu$ m by chemical etching. By neglecting these small bumps the simple model shown in Fig. 1 can be applied in our experimental arrangement. Here  $d_1 + d_2 = d_2 + d_3 = 10$   $\mu$ m,  $t_1 = 0.04$   $\mu$ m,  $t_3 = 1.6$   $\mu$ m and  $d_2$  is estimated to be 1  $\mu$ m.

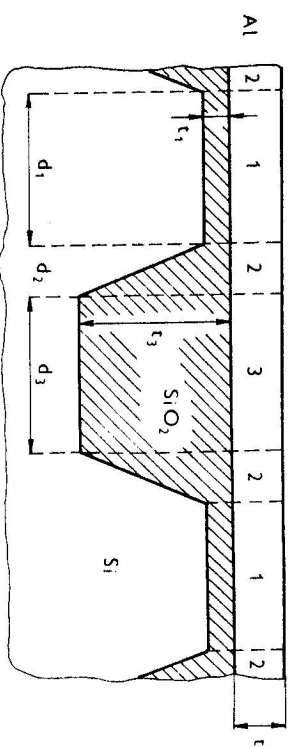


Fig. 1. The simplified model of the sample with varying thickness of the silicon oxide

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Test conductors with four expanded contacts (Fig. 2) were patterned photolithographically in Al-Cu-Si films on both types of substrates. The length and width of stripes were  $l = 400 \mu\text{m}$  and  $w = 6.5 \mu\text{m}$ , respectively. The conductors were passivated by PE CVD silicon nitride  $0.9 \mu\text{m}$  thick, deposited at  $380^\circ\text{C}$ . They were bonded ultrasonically by aluminium wires and the samples were completed by encapsulating the chips into ceramic packages.

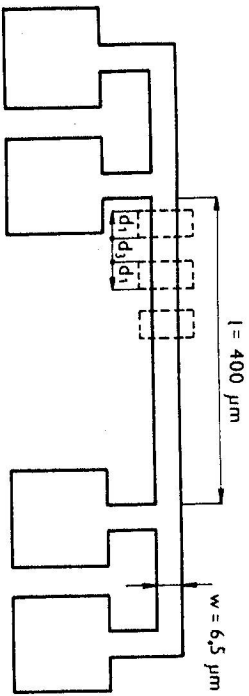


Fig. 2. The conductor on the substrate with varying thickness of the silicon oxide

Due to four contacts the resistivity of conductors can be measured and the samples can be used as self-thermometers for the evaluation of their own temperature

$$g = g_0 + \Delta g. \quad (1)$$

Here  $g_0$  is the temperature of the ambient (oven, thermostat) and  $\Delta g$  is the temperature increase due to Joule heating, which follows from the simple relation  $R = R_0(1 + \alpha\Delta g)$ . ( $R$  is the resistance of the conductor and  $\alpha$  is the temperature coefficient of resistance, which is measured independently at small current density  $< 10^6 \text{ A/cm}^2$ .)

The temperature increase  $\Delta g$  at  $j > 10^6 \text{ A/cm}^2$  was measured at a.c. stressing (50 Hz) with the effective current value  $I_{ef} = j/w$ , where  $l$  is the metallic film thickness. This procedure must be employed because it was observed that at conventional d.c. stressing the results are influenced by electromigration defect formation during long measuring cycles, caused by the thermal inertia of the samples.

### 3. RESULTS AND DISCUSSION

The resistivity and the temperature coefficient of resistance of conductors under investigation are  $\rho_{20^\circ\text{C}} = 4.7 \mu\text{ Ohm cm}$  and  $\alpha = 2300 \times 10^{-6} \text{ K}^{-1}$  (for  $20 - 250^\circ\text{C}$ ), respectively. The increase of the temperature  $\Delta g$  was measured at  $g_0 = 180^\circ\text{C}$  and  $I_{ef} = 140 \text{ mA}$  ( $j = 3.6 \times 10^6 \text{ A/cm}^2$ ).

In the case of the conductor on a planar surface the values  $\Delta g = 69 - 71^\circ\text{C}$  were obtained with five samples, the mean value being  $\overline{\Delta g} = 70^\circ\text{C}$  and  $\bar{g} = 250^\circ\text{C}$ .

In our preceding experiments with similar samples it was shown [4] that the dependence between  $\Delta g$  and the power dissipated in the conductor is linear:

$$\Delta g = \gamma R(g) I_{ef}^2 = \gamma W. \quad (2)$$

Here  $W$  is the input power and  $\gamma$  is the slope which did not depend on the ambient temperature in the used interval of  $g_0 = 30 - 180^\circ\text{C}$ . The relation (2) was verified for  $j = (1 - 4) \times 10^6 \text{ A/cm}^2$  and the values  $\Delta g$  were  $\leq 100^\circ\text{C}$ .

The simple calculation, with the boundary Si — SiO<sub>2</sub> assumed to be the isothermal surface with the temperature  $g_0$ , yields

$$\gamma = \frac{I_{\text{SiO}_2}}{K_{\text{SiO}_2} l w}. \quad (3)$$

For our samples  $\gamma = 462 \text{ K/W}$ . This value can be compared with the experimental one, obtained from the relation (2), where  $\overline{\Delta g} = 70^\circ\text{C}$  and  $R$  is calculated by means of the resistivity  $\rho_{250^\circ\text{C}} = 7.2 \times 10^{-6} \mu\text{ Ohm cm}$ . Then  $W = 145 \text{ mW}$  and  $\gamma_{\text{exp}} = 483 \text{ K/W}$ . The difference between both slopes is quite small with regard to the simplified model and to the temperature drops on the chip and the package, respectively.

Measurements of a similar type were performed by Fischer and Neppi [8, 9]. In their papers the input power  $W$  and the current induced temperature rise  $\Delta g$  are related using the quantity  $h = W/lw\Delta g$ , called heat transfer rate. The exact comparison of these and our results was not possible because not all relevant data were found in papers [8, 9]. It could be only estimated that the results differ less than within the factor of 3.

In the case of conductors on chips with varying SiO<sub>2</sub> thickness the values  $\Delta g = 37 - 39^\circ\text{C}$  ( $\overline{\Delta g} = 38^\circ\text{C}$ ,  $\bar{g} = 218^\circ\text{C}$ ) were obtained with five samples. In this case  $\Delta g$  represents some average value and the temperature along the conductor fluctuates about this level. It is important to know the amplitude of these fluctuations in order to estimate the temperature gradients in the conductor, which adversely influence the electromigration reliability and lifetime of the metallization. The direct measurement of the temperature distribution was beyond our possibilities, therefore we tried to throw some light upon this problem by approximate calculations at least.

#### 4. DISTRIBUTION OF TEMPERATURE ALONG THE CONDUCTOR CROSSING THE REGIONS WITH VARYING SiO<sub>2</sub> THICKNESS

We use the model shown in Fig. 1. Here the passivation layer is omitted with regard to its thermal conductivity, which is approx. 20 times smaller than that of aluminium [10]. We assume that the temperature at the Si — SiO<sub>2</sub> boundary equals  $\vartheta_0$ .

The analysis of the chosen model is based on the heat balance of three Al-Cu-Si segments according to Fig. 1. The mean temperatures of the individual conductor segments  $i = 1, 2, 3$  are  $\vartheta_i$ , Joule heats dissipated in the corresponding parts of the conductor are  $Q_i$ , and  $P_i$  represent the heats conducted perpendicularly through the oxide into the substrate. Finally,  $T_{21}$  and  $T_{32}$  are heats exchanged between the indicated segments. Further, we assume a two-dimensional configuration, i.e. the constant temperature across the width of the conductor.

In thermal equilibrium  $T_2 = -T_1$  and  $T_3 = -T_2$  and the heat balance in each segment gives

$$Q_1 = P_1 - 2T_{21}, \quad (4)$$

$$Q_2 = P_2 + T_{21} - T_{32}, \quad (5)$$

$$Q_3 = P_3 + 2T_{32}. \quad (6)$$

The mean distances of segments from the Si — SiO<sub>2</sub> boundary are

$$l_1 = l_1 + \frac{l}{2}, \quad (7)$$

$$l_2 = \frac{l_1 + l_3 + l}{2}, \quad (8)$$

$$l_3 = l_3 + \frac{l}{2}. \quad (9)$$

Dissipated Joule heat is given by

$$Q_i = \frac{\varrho(\vartheta_i) I^2 d_i}{wt} \quad (10)$$

and for the conducted heats  $P_1, T_{21}, T_{32}$  one can use the linear estimates

$$P_i = \frac{\lambda_{\text{SiO}_2}(\vartheta_i - \vartheta_0) d_i w}{l_i}, \quad (11)$$

where  $\lambda_w$  is the thermal conductivity of the metallization.

Using the experimental values  $\lambda_w = \lambda_{\text{Al}}$ ,  $\varrho(\vartheta) = \varrho(218^\circ\text{C}) = 6.85 \mu\text{Ohm cm}$  (here the small temperature differences between resistivities of individual segments were omitted) and others mentioned above, we evaluate the segment temperatures:  $\vartheta_1 - \vartheta_0 = 22.5^\circ\text{C}$ ,  $\vartheta_2 - \vartheta_0 = 28^\circ\text{C}$ ,  $\vartheta_3 - \vartheta_0 = 32^\circ\text{C}$ .

The experimental value  $\Delta\vartheta = 37\text{--}39^\circ\text{C}$  (chap. 3) can be compared with the calculated mean temperature increase of the conductor. With regard to the predominant influence of segments 1 and 3 this quantity can be expressed as  $(\vartheta_1 + \vartheta_3)/2 - \vartheta_0 = 27.25^\circ\text{C}$ . Hence, the agreement is quite good, having in mind the temperature drop on the semiconductor and the ceramic parts of the sample.

According to our calculations the temperature differences of  $\approx 10\text{K}$  and the temperature gradients  $2(\vartheta_3 - \vartheta_1)/(d_1 + d_3 + 2d_2) \approx 10^4\text{K/cm}$  are to be expected in the investigated conductors. These values are quite high and they are comparable with those reported in ref. [6]. Consequently, the electromigration voids and hillocks can form in the places where the thickness of the oxide changes abruptly.

In our calculations the quantity  $\lambda_w = \lambda_{\text{Al}}$  was used, as the exact value of  $\lambda_{\text{Al-Cu-Si}}$  and its temperature dependence could not be measured. Using the Wiedemann—Franz law it can be estimated that  $\lambda_{\text{Al-Cu-Si}}$  equals approx.  $1.7\text{W/cm K}$  at  $218^\circ\text{C}$ . However, even this shift of thermal conductivity does not influence the calculated temperatures markedly. The temperatures  $\vartheta_i$  are slightly higher, the increase being  $\approx 3.5^\circ\text{C}$ , and  $(\vartheta_1 + \vartheta_3)/2 - \vartheta_0 \approx 29^\circ\text{C}$ . The differences correlate with decreased heat exchange between the segments.

#### 5. CONCLUSIONS

It was shown that the increase of the temperature of metallization of silicon devices due to the dissipation of the Joule heat is influenced first of all by the thickness of the SiO<sub>2</sub> underlayer, which is a bad heat conductor. On the other hand, the thermal conductivity of the silicon substrate is high. Therefore, the heating of metallization can be estimated with sufficient accuracy by the use of very simple models and procedures, which yield the distribution of temperature in two-dimensional and two-layered structures. Further, it follows from the paper that attention should be devoted to the temperature activated degradation processes and the operational stability of tomorrow's semiconductor devices and circuits with narrow conductors, carrying high current densities.

## REFERENCES

- [1] D'Heurle, F. M., Ho, P. S.: In: *Thin Films-Interdiffusion and Reactions*. (Eds. J. M. Poate, K. N. Tu, J. W. Mayer). J. Wiley, New York 1978, p. 243.
- [2] Hartsough, L. D., Denison, D. R.: *Solid State Technol.*, 22 (1979), No. 12, 66.
- [3] Vaidya, S., Fraser, D. V., Lindenberger, W. S.: *J. Appl. Phys.* 51 (1980), 4475.
- [4] Luby, Š., Roman, P., Vargha, P. V.: *Elektrotechn. čas.*, 35 (1984), 298.
- [5] Luby, Š., Loboika, P.: *Elektrotechn. čas.*, 30 (1979), 409.
- [6] Luby, Š. et al.: *Stabopr. obzor* 40 (1979), 201.
- [7] Ghate, P. B.: *Solid State Technol.* 26 (1983), No. 3, 113.
- [8] Fisher, F.: *Siemens Forsch.-u. Entwickl. Ber.* Bd. 13, No 1, Springer Verlag 1984, p. 21.
- [9] Fischer, F., Nerpl, F.: *Proc. 22nd Annual Int. Reliability Symp.* 1988, IEEE, New York 1984, p. 190.
- [10] Wilson, A. M.: *Thin Solid Films* 23 (1981), 145.

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## ВЛИЯНИЕ НИЖНЕГО СЛОЯ SiO<sub>2</sub> НА ДЖОУЛЕВСКОЕ НАГРЕВАНИЕ Al-Cu-Si МЕТАЛЛИЗАЦИИ КРЕМНИЕВЫХ ПРИБОРОВ

Экспериментальные проводники приготовались в Al-Cu-Si пленках, нанесенных магнетронным напылением на окисленные кремниевые подложки как с постоянной, так и с меняющейся толщиной SiO<sub>2</sub>. Проводники загружались высокой плотностью тока ( $> 10^6$  А/см<sup>2</sup>). При этих условиях повышение температуры проводников, обусловленное джоулевским нагреванием, достигало 70 °С для первого типа подложки. Для подложки с переменной толщиной окисла, где толщина была не больше, чем в первом случае, среднее значение повышения температуры (флуктуирующей вдоль проводника), было 37—39 °С. Экспериментальные результаты сравнены с расчетами распределения температуры, основанного на простой модели. Соответствие довольно хорошее; это подкажывает, что на нагревание в металлизации влияет главным образом толщина нижнего слоя SiO<sub>2</sub>, температура проводимости которого на два порядка ниже, чем у кремния. Результаты демонстрируют, что высокие плотности тока могут существенно повлиять на действие и надежность полупроводниковых приборов.